Integrated 4-bit Optical Memory Elements with Single Common and Low Operation Current (55mA) Using Novel Active MMI

H. A. Bastawrous, H. Jiang, Y. Tahara, T. Hagio, and K. Hamamoto

Optical random access memory (RAM) is a key device for realizing all-optical routers especially as a buffering function. To realize highly integrated optical memory elements, common single-current driving condition is desired for all the integrated devices even in case of their further downsizing. In this report, we demonstrate relatively low operation current of 55mA with maintaining wide hysteresis window width of 10mA (approx. 20% of operation current) for 4-bit memory elements. To realize wide hysteresis window even in the case of downsizing of the device, we have proposed a novel principle based on active-MMI BLDs utilizing different lateral modes with sharing exactly same port at one facet side (as shown in Fig. 1) [1]- [4]. This schema offers superior controllability in the portion of cross-gain saturation region, which leads to wide hysteresis window that allows common single-current driving for the integrated devices. Moreover, we designed to increase the cross-gain saturation overlap portion between 0^{th} mode and 1^{st} mode by 5% compared to our previous design [1]. Figure 2 shows microscopic top photograph of integrated 4-bit optical memory elements. We used ridge waveguide structure with 1.55μm InGaAsP/InGaAsP multiple-quantum well (7 layers), and MMI region was designed to have a width of W_{MMI} = 7.4μm and a length of L_{MMI} = 123μm. Total length of the device was 355μm including saturable absorber section of 50μm. In Fig. 3, we illustrate the power-current characteristics of the integrated 4-bit optical memory elements. As we can see from the figure, at least 10mA hysteresis window for all the elements was realized at similar threshold currents (approx. from 50mA to 60mA). These relatively low hysteresis threshold currents were mainly due to device-size reduction with relatively short saturable absorber section. As the cross-gain saturation region was designed to have 5% increase, not to lose sufficient bi-stable hysteresis window, we could confirm 20% hysteresis window of the operation current although the device size was designed with 40% size reduction and relatively short saturable absorber section. For the switching characteristics evaluation, input energy as low as 0.3pJ was injected (@λ=1.56μm) with using a single common operation current of 55mA to all the 4-bit memory elements. This work was supported in part by NICT, Japan.

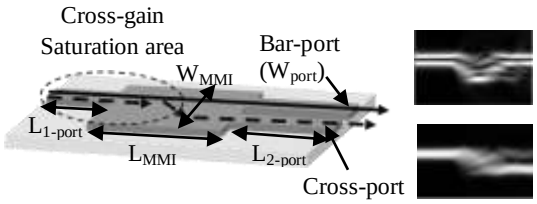

Figure 1 Schematics of novel active-MMI BLDs (circle indicates cross-gain saturation region).

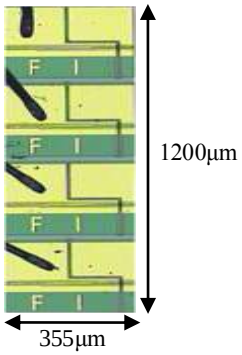

Figure 2 Microscopic top photograph of integrated 4-bit optical memory elements

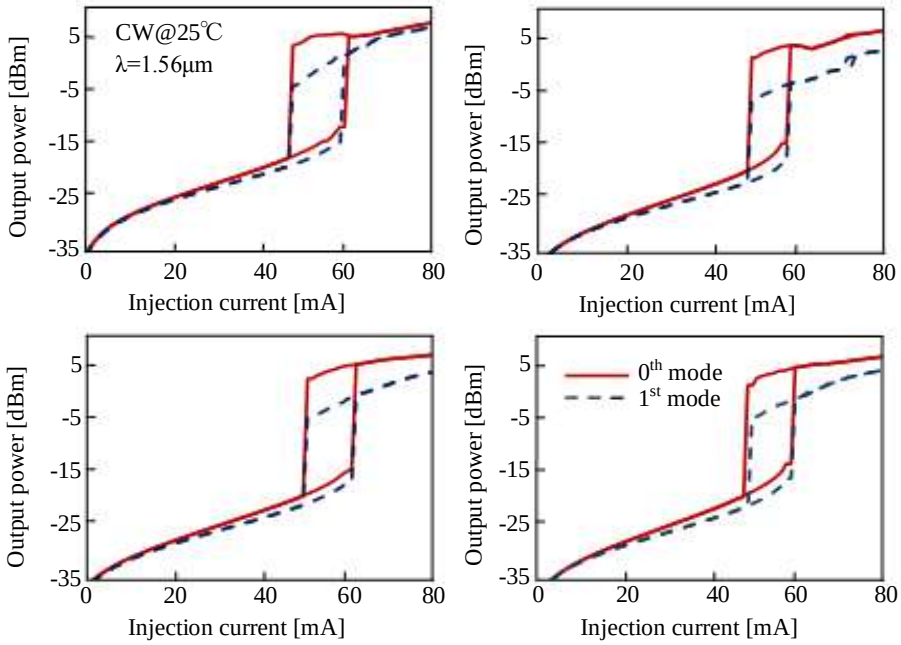

Figure 3 Static hysteresis characteristics for the 4-bit optical memory

References
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[2] H. A. Bastawrous et al., Proc. OFC2009, OTuK2.
[3] H. A. Bastawrous et al., Proc. ECOC2009, P.2.15.
[4] H. Jiang et al, in Techn. Dig. 15th MOC, G5 (2009).